IN THE SPECIFICATION:

Please amend paragraph number **[0002]** as follows:

[0002] Field of the Invention: The present invention relates to an apparatus and a method for increasing semiconductor device density. In particular, the present invention relates to a stacked multi-substrate device using a combination of ~~flip chips~~ flip-chips and chip-on-board assembly techniques to achieve densely packaged semiconductor devices.

Please amend paragraph number **[0003]** as follows:

[0003] State of the Art: Chip-On-Board techniques are used to attach semiconductor dice to a printed circuit board, including flip-chip attachment, wirebonding, and tape automated bonding ("TAB"). Flip-chip attachment consists of attaching a ~~flip chip~~ flip-chip to a printed circuit board or other substrate. A ~~flip chip~~ flip-chip is a semiconductor chip that has a pattern or array of electrical terminations or bond pads spaced around an active surface of the ~~flip chip~~ flip-chip for face down mounting of the ~~flip chip~~ flip-chip to a substrate. Generally, the ~~flip chip~~ flip-chip has an active surface having one of the following electrical connectors: Ball Grid Array ~~("BGA") wherein~~ ("BGA"), wherein an array of minute solder balls is disposed on the surface of a ~~flip chip~~ flip-chip that attaches to the substrate ("the attachment surface"); Slightly Larger than Integrated Circuit Carrier ~~("SLICC") which~~ ("SLICC"), which is similar to a BGA, but having a smaller solder ball pitch and diameter than a BGA; or a Pin Grid Array ~~("PGA") wherein~~ ("PGA"), wherein an array of small pins extends substantially perpendicularly from the attachment surface of a ~~flip chip.~~ flip-chip. The pins conform to a specific arrangement on a printed circuit board or other substrate for attachment thereto. With the BGA or SLICC, the solder or other conductive ball arrangement on the ~~flip chip~~ flip-chip must be a mirror-image of the connecting bond pads on the printed circuit board such that precise connection is made. The ~~flip chip~~ flip-chip is bonded to the printed circuit board by refluxing the solder balls. The solder balls may also be replaced with a conductive polymer. With the PGA, the pin arrangement of the ~~flip chip~~ flip-chip must be a mirror-image of the pin recesses on the printed circuit board. After insertion, the ~~flip chip~~ flip-chip is generally bonded by

soldering the pins into place. An under-fill encapsulant is generally disposed between the ~~flip chip~~ flip-chip and the printed circuit board for environmental protection and to enhance the attachment of the ~~flip chip~~ flip-chip to the printed circuit board. A variation of the pin-in-recess PGA is a J-lead PGA, wherein the loops of the J's are soldered to pads on the surface of the circuit board.

Please amend paragraph number **[0004]** as follows:

[0004] Wirebonding and TAB attachment generally begin with attaching a semiconductor chip to the surface of a printed circuit board with an appropriate adhesive, such as an epoxy. In wirebonding, bond wires are attached, one at a time, to each bond pad on the semiconductor chip and extend to a corresponding lead or trace end on the printed circuit board. The bond wires are generally attached through one of three industry-standard wirebonding techniques: ultrasonic ~~bonding - using~~ bonding, using a combination of pressure and ultrasonic vibration bursts to form a metallurgical cold weld; thermocompression ~~bonding - using~~ bonding, using a combination of pressure and elevated temperature to form a weld; and thermosonic ~~bonding - using~~ bonding, using a combination of pressure, elevated temperature, and ultrasonic vibration bursts. The semiconductor chip may be oriented either face up or face down (with its active surface and bond pads either up or down with respect to the circuit board) for wire bonding, although face up orientation is more common. With TAB, ends of metal leads carried on an insulating tape, such as a polyamide, are respectively attached to the bond pads on the semiconductor chip and to the lead or trace ends on the printed circuit board. An encapsulant is generally used to cover the bond wires and metal tape leads to prevent contamination.

Please amend paragraph number **[0014]** as follows:

[0014] As has been illustrated, none of the cited prior art above uses or teaches ~~flip chip~~ flip-chip manufacturing methods for attaching dice together in a stacked manner to form a stacked die assembly.

Please amend paragraph number **[0015]** as follows:

[0015] Therefore, it would be advantageous to develop a stacking technique and assembly for increasing integrated circuit density using a variety of non-customized die configurations in combination with ~~commercially available, widely practiced~~ commercially available, widely practiced semiconductor device fabrication techniques.

Please amend paragraph number **[0016]** as follows:

[0016] The present invention relates to a stacked multi-substrate device using combined ~~flip chips~~ flip-chips and chip-on-board assembly techniques to achieve densely packaged semiconductor devices, and a method for making same. In this invention, multiple substrates are stacked atop one another. The substrates can include a plurality of semiconductor dice disposed on either surface of the substrates. The substrates can be structures of planar non-conductive material, such as fiberglass material used for PCBs, or may even be semiconductor dice. For the sake of clarity, the term "substrate," as used hereinafter, will be defined to include planar non-conductive materials and semiconductor dice. The substrates are preferably stacked atop one another by electric connections which are ball or column-like structures. Alternately, solder bumps or balls may be formed on the substrate. The electric connections achieve electric communication between the stacked substrates. The electric connections can be formed from industry standard solder forming techniques or from other known materials and techniques, such as conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, TAB tape, and the like. The electric connections must be of sufficient height to give clearance for the components mounted on the substrates and should be sufficiently strong enough to give support between the stacked substrates.

Please amend paragraph number **[0017]** as follows:

[0017] A preferred embodiment comprises a base substrate, having first and opposing surfaces, and means for electrical connection with external components or substrates, wherein the electrical connection means extends at least from the first surface of the base substrate. The base

substrate opposing surface, the other side of the substrate, also includes a plurality of bond pads disposed thereon. Additionally, at least one semiconductor component may be attached to the opposing surface of the base substrate. The semiconductor components are preferably ~~flip-chips~~ flip-chips that are in electrical communication with electrical traces on or within the base substrate with any convenient known chip-on-board (COB) or direct-chip-attachment (DCA) technique (i.e., flip-chip attachment, wirebonding, and TAB). Other techniques, such as the use of two-axis materials or conductive epoxies, can also be used for connections between either substrates or substrates and semiconductor chips. The electrical traces form a network of predetermined electrical connections between the base substrate electrical connection means, the base substrate bond pads, and/or the base substrate semiconductor components.

Please amend paragraph number **[0018]** as follows:

[0018] The preferred embodiment further comprises a stacked substrate. The stacked substrate has a first surface and an opposing surface. A plurality of bond pads may be disposed on the stacked substrate first surface and/or the stacked substrate opposing surface. At least one semiconductor component is attached to each of the stacked substrate first surface and the stacked substrate opposing surface. The semiconductor components are preferably ~~flip-chips~~ flip-chips which are in electrical communication with electrical traces on or within the first stacked substrate. The electrical traces form a network of predetermined electrical connections between the stacked substrate first surface bond pads, the stacked substrate opposing surface bond pads, and/or the stacked substrate semiconductor components.

Please amend paragraph number **[0035]** as follows:

[0035] A plurality of second semiconductor dice ~~150~~ 150, each having a face side 152 and a back side ~~154~~ 154, is attached to the second stacked substrate first surface 142 with a second layer of adhesive 156 applied to the second semiconductor die back sides 154. The second semiconductor dice 150 are in electrical contact with a plurality of second stacked substrate electrical traces 158 via wirebonds 160. A plurality of third semiconductor dice 162

each having a face side 164 is attached to the second stacked substrate second surface 146 with a plurality of flip-chip contacts 166, such as BGA, PGA or the like. The flip-chip contacts 166 are in electrical contact with the second stacked substrate electrical traces 158. The second stacked substrate electrical traces 158 extend in or on the second stacked substrate 140 and may contact the second stacked substrate first surface bond pads 144, the second semiconductor dice 150 and/or another third semiconductor die 162.

Please amend paragraph number **[0043]** as follows:

[0043] A plurality of third semiconductor dice ~~452~~ 452, each having a face side 454 and a back side ~~456~~ 456, is attached to the second stacked substrate second surface 446 with a third layer of dielectric adhesive 458 applied to the third semiconductor die back sides 456. The third semiconductor dice 452 are in electric communication with a plurality of second stacked substrate electrical traces (not shown) via wirebonds 460.

Please amend paragraph number **[0045]** as follows:

[0045] A plurality of fourth semiconductor dice ~~474~~ 474, each having a face side 476 and a back side ~~478~~ 478, is attached to the third stacked substrate first surface 464 with a fourth layer of dielectric adhesive 480 applied to the fourth semiconductor die back sides 478. The fourth semiconductor dice 474 are in electrical contact with a plurality of third stacked substrate electrical traces (not shown) via wirebonds 482. A plurality of fifth semiconductor dice ~~484~~ 484, each having a face side 486 and a back side ~~488~~ 488, is attached to the third stacked substrate second surface 468 with a fifth layer of dielectric adhesive 490 applied to the fifth semiconductor die back sides 488. The fifth semiconductor dice 484 are in electric communication with a plurality of third stacked substrate electrical traces (not shown) via wirebonds 492.

Please amend paragraph number **[0048]** as follows:

[0048] FIG. 6 illustrates a substrate assembly 700 having a plurality of semiconductor devices mounted on substrates using known flip-chip attachment techniques. The substrate assembly 700 comprises a first substrate 704 having a plurality of first semiconductor dice 702 disposed thereon and a second substrate 708 having a plurality of second semiconductor dice 706 disposed thereon. The first semiconductor dice 702 each have a surface or face side 710 having a plurality of bond pads (not shown) thereon and a back side 712. The first semiconductor dice 702 make electrical contact with the traces (not shown) on the first substrate surface 714 by a plurality of first conductive material balls 716 extending between the bond pads (not shown) on the face surface 710 of the dice 702 and the traces (not shown) on the first substrate surface 714. The balls 716 may be made of any suitable conductive material to connect the semiconductor dice 702 to the conductive traces on first substrate 704, such as solder, conductive epoxy, etc. The balls 716 are shown as generally spherical in shape, although they may be any suitable geometric shape and size for bonding purposes. Further, z-axis connectors may be substituted for the balls 716 if so desired. The second substrate 708 has a surface 718 having a plurality of conductive traces (not shown) thereon. The second plurality of semiconductor dice 706 each have a face side 720 having a plurality of bond pads (not shown) thereon and a back side 722. The second plurality of semiconductor dice 706 make electrical contact with the second substrate surface 718 by a plurality of second conductive material balls 724 extending between the bond pads of the dice 706 and the conductive traces on the second substrate surface 718. The balls 724 may be made of any suitable conductive material to connect the semiconductor dice 706 to the conductive traces on second substrate 708, such as solder, conductive epoxy, etc. The balls 724 are shown as generally spherical in shape, although they may be any suitable geometric shape and size for bonding purposes. Further, z-axis connectors may be substituted for balls 724 if so desired. The desired conductive traces on the surface 714 of the first substrate 704 are connected to the desired conductive traces on the surface 718 of the second substrate 708 by larger conductive balls 726. The larger conductive balls 726 may be of any suitable conductive material, such as solder, conductive epoxy, etc. The larger conductive balls are also used for

connecting the surface 728 of the first substrate 704 to any other desired substrate. Further, z-axis connectors may be substituted for balls 726 if so desired. It should be understood that the conductive traces which have only been referred to on the surfaces 714 and 718 of the substrates may be formed on either side of the first substrate 704 or the second substrate 708 and, as such, have not been illustrated. Also, any connectors extending through the first substrate 704 and second substrate 708 for connection purposes have not been shown. Similarly, the bond pads on the first semiconductor dice 702 and second semiconductor dice 706 have not been illustrated. The first semiconductor dice 702 are attached to the first substrate 704 and the second semiconductor dice 706 are attached to the second substrate 708 by well known ~~flip chip~~ flip-chip bonding techniques, depending upon the type of conductive balls 716 and 724 used for connection purposes.